PSpice Investigation of Bridge Transistor CFI Supplied from Hysteresis Current Controlled BUCK DC-DC Regulator

Georgi Tzvetanov Kunov, Georgi Hristov Gigov and Mario Zhekov Metodiev

Abstract - **In the present paper, the work of a stand alone current fed inverter, as well as the work of a current fed inverter together with a DC-DC BUCK regulator, is investugated, with application in the induction heating technologies. Using the program package *PSpice*, the work of the hysteresis current controlled DC-DC BUCK regulator as a current source with variable load is sumulated. The commutation processes are investigated in a full bridge current fed inverter working by capacitance as well as by inductance detuning of the load resonant circuit.**

Keywords –**Power electronics, CF invertors, Induction heating, Tube welding, PSpice simulation, Transient analysis.**

I. INTRODUCTION

In the field of induction electro-technologies, depending on the working frequency and power, widespread application have the circuits of full bridge thyristor and transistor series resonant inverters or parallel current fed inverters (CFI) [1-7]. It is accepted that the series inverters are fed from a voltage source and the parallel inverters – from a current source. The following specific feature exists by the parallel inverters: according to the theory, the voltage on the load and on the semiconductor devices is expressed by the supply voltage V_{dc} and by the detuning angle of the resonant circuit:

$$V_{load} = \frac{\sqrt{2}V_{dc}}{0.9\cos\beta} \qquad (1)$$

This is due to the fact that the DC power supply of the inverter is ensured by a thyristor rectifier. The filter inductor in its output circuit plays the role of a current source for the inverter. The value of this current, however, depends on the voltage, submitted from the rectifier. With the occurrence of power MOSFET and IGBT transistors, the combination of diode rectifier and DC-DC BUCK regulator is used for the power supply of the inverters. The application of the principle of the hysteresis current control makes them an ideal current source for a wide range of the load variation (from a short circuit to the nominal load).

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This specific feature allows current overload-protection of the parallel inverter.

The voltage on the resonant circuit of the parallel inverter can be regulated by the current value of the DC-DC regulator, as well as by a variation of the working frequency.

II. DC-DC BUCK REGULATOR

The simulated circuit of the DC-DC regulator is shown in Fig. 1. The investigation is performed by the program package *Cadence PSpice* [10]. The current through the load resistor R_{load} is monitored by the current-to-voltage converter H1. The output signal is submitted simultaneously to the inputs IN- and IN+ of the comparators EL1 and EL2. The switching levels of the comparators are determined by the divider RL1/RL2, to which the voltage VIref (the reference for the desired load current) is applied. The RS flip-flop (U1A, U2A) commutates the transistor Qbuck of the DC-DC regulator.

The simulation of the circuit is performed for four values of the load current (5A, 20A, 40A and 60A) and two values of the load resistor 1 Ω and 10 Ω. The results of the parametric analysis are shown in Fig. 2.

It is seen, that despite of the R_{load} value, the DC-DC regulator behaves as a ideal current source. The commutation frequency of the transistor depends on the time constant $\tau = L_{dc}/R_{load}$.

The decreasing the R_{load} value leads to increasing the time constant τ and to decreasing the commutation frequency.

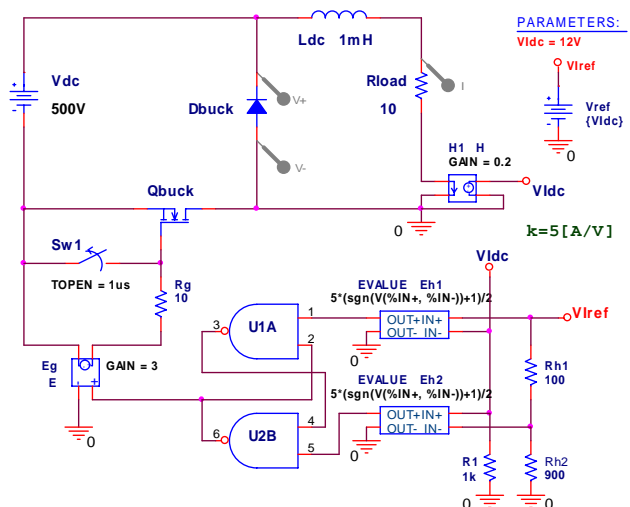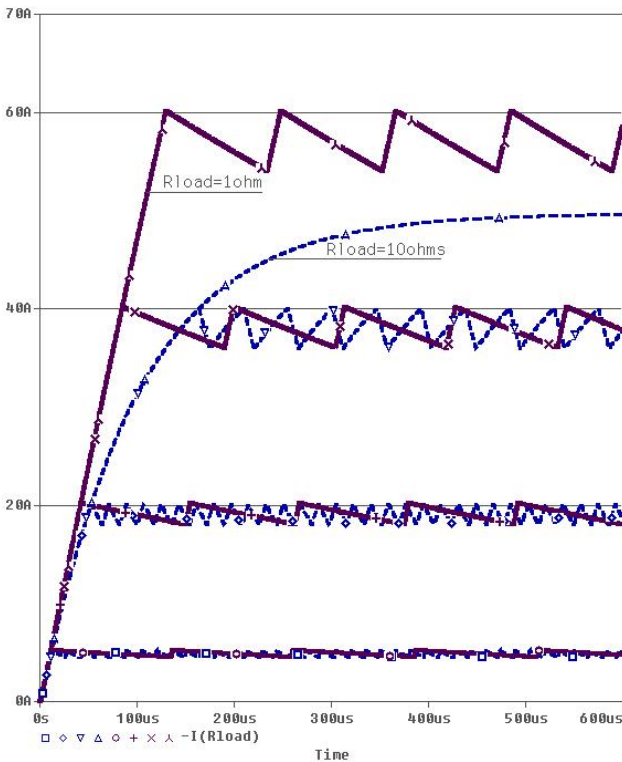

Fig.1. DC-DC BUCK regulator

Fig. 2. Waveforms of the load current of the DC-DC BUCK regulator

The increasing of the reference VIref for desired load current over the maximal value, limited by the value of R_{load}, leads to a mode, when the transistor is constantly ON.

III. CURRENT FED INVERTER

A. Frequency characteristic of the inverter

The circuit of the parallel full bridge transistor inverter, supplied by ideal current source, is shown in Fig. 3. Using the *Cadence PSpice*, the dependence of the voltage across the resonant circuit is investigated, as a function of the commutation frequency of the transistors. The same dependence is also investigated using the equivalent circuit shown in Fig. 4. In the equivalent circuit, the source of rectangle current I_{ac} corresponds to the current in the diagonal of the inverter (I_{Rcs}). The results of both simulations are shown in Fig. 5. It is seen that the shape of the frequency dependence of the voltage on the resonant circuit of the inverter, supplied by DC current source, coincides with that for the module of its impedance. The following conclusions can be made, based on this result:

1. By the design of the inverter, the equivalent resonant resistance of the resonant circuit

$$R_{e0} = \frac{L_{ind}}{R_{ind} C_{ind}}, \qquad (2)$$

has to be of such value, so that the DC-DC regulator can ensure the nominal current to supply the inverter, corresponding to the desired load power;

2. By the work in the mode of nominal current and fast increasing of the equivalent resistance of the resonant circuit, overvoltages will appear on the load and on the transistors.
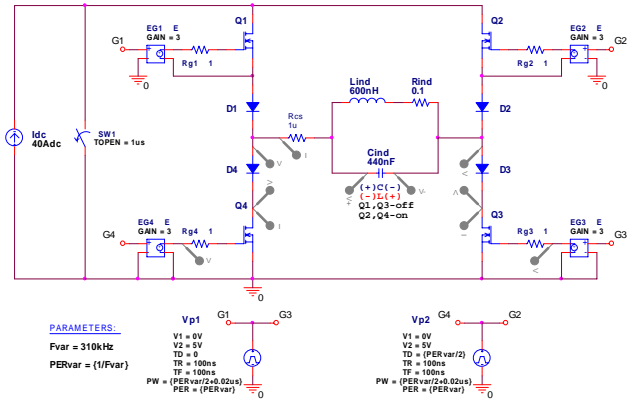

Fig. 3. Parallel full bridge transistor inverter, supplied by ideal current source
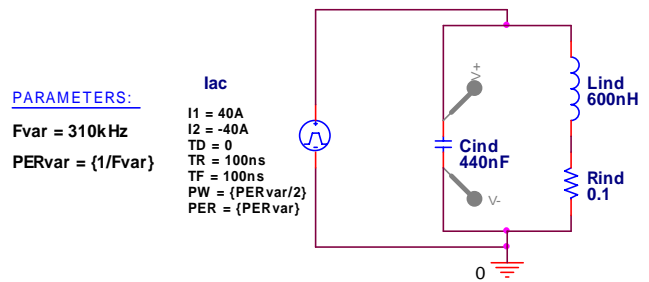

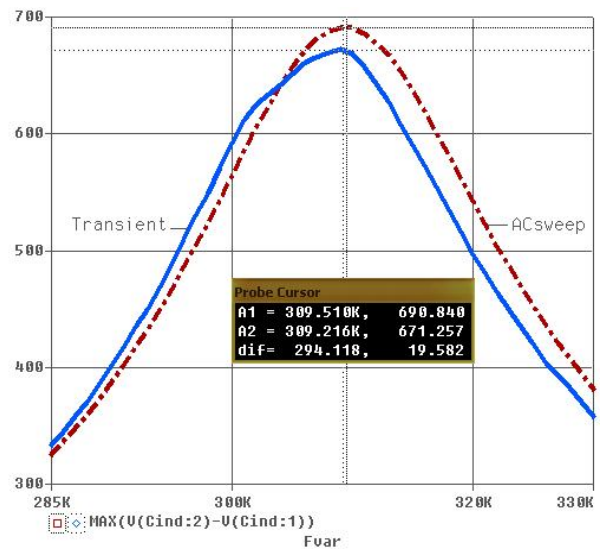Fig. 4. Equivalent circuit with the current source I_{ac}

Fig. 5. The dependence of the voltage across the resonant circuit as a function of the commutation frequency

In practice, such mode of operation could be obtained in the case of induction tube welding [8]. This failure mode of operation can be avoided by increasing the detuning of the resonant circuit.

B. Commutation processes by capacitance and inductance detuning of the resonant circuit

According to the resonant frequency of the resonant circuit, the current fed inverter can operate at a lower frequency (inductance detuning), at the same frequency (in a resonance) or at a higher frequency (capacitance detuning).
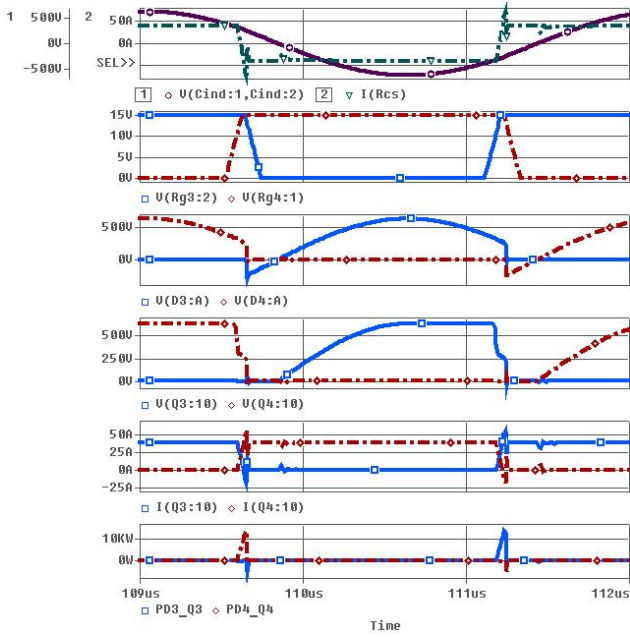
Fig. 6. The waveforms in the mode of capacitance detuning

Fig.7. The waveforms in the mode of inductance detuning

Following the requirement for the maximum power transfer, by a nominal current supply, the work at the resonant frequency is preferable. This is seen from the frequency characteristic, presented in Fig. 5.

In practice, the mode of operation is chosen, taking into account the commutation processes in the transistors and the commutation losses connected with these processes. From the point of view of so called soft switching by the transistor inverters, the inductance type of the load is preferable [9]. In the case of fast variation of the equivalent resistance of the resonant circuit, the inverter can pass from one node of operation to another. Therefore, both modes will be considered – by capacitance and by inductance detuning.

The waveforms in the mode of capacitance detuning are shown in Fig. 6. From the top to the bottom the following characteristics are arranged: the current I_{Rcs} through the inverter diagonal and the voltage on the resonant circuit; the control impulses for the odd and even transistors V_{Rg3} and V_{Rg4}; the voltage on the connected in series diode and transistor (D_3, Q_3) and (D_4, Q_4); the voltage on the transistors Q_3 and Q_4; the current through the transistors Q_3 and Q_4, and the dissipated power in the transistors Q_3 and Q_4 during their commutation. In this mode the commutation processes in the transistor CFI are similar to these in the thyristor inverter. The inverter voltage lags behind the inverter current. In the turn-on moment of the successive diode-transistor pair, a negative voltage is applied to the previous diode-transistor pair. The commutation power on (D_4, Q_4) (denoted as PD4_Q4 in Fig. 6) has its maximum during their turn-on. In this moment a peak current is flowing through them, larger than the current I_{Rcs}. It is a result of the reverse current for the time interval t_{rr}. During this interval a negative voltage is applied to the previous pair diode-transistor (D_3, Q_3), which are turn-off. There exists a dissipated power PD3_Q3 on this pair as well. It is presented in Fig. 6 with a negative value.
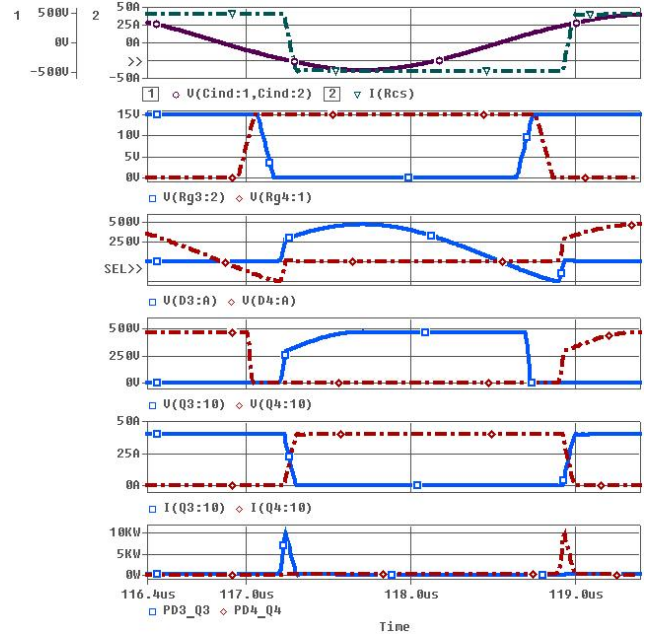
As it is seen from the waveforms, commutation losses exist on the devices in this mode during the turn-on (P_{on}) and during the turn-off (P_{off}). The losses P_{on} are dominating.

The waveforms in the mode of inductance detuning are shown in Fig. 7. The inverter current lags behind the inverter voltage. In the turn-on moment of the successive diode-transistor pair, the voltage on it has a negative value (for example (D_4, Q_4)).

The transistor Q_4 is turn-on, but the current through this transistor starts to flow even then the previous transistor Q_3 is turn-off. It is seen, that in this mode of operation, the conditions for commutation by zero current (ZCS) are satisfied. In the moment of turn-off of the transistor Q_3, the voltage on the pair (D_3, Q_3) is positive. Therefore, a reverse recovery current I_{rr} does not flow though the diode D_3. Due to the existing ZCS there is no P_{on}. In this mode of operation of CFI only P_{off} exists. Its peak value is significantly smaller than P_{on} by capacitance detuning.

The result from the investigation of the transients in the working together hysteresis current controlled DC-DC BUCK regulator and CFI, are shown in Fig. 8. The time for reaching the steady state, the pulse frequency of the supply current I_{dc}, of the inverter current I_{Rcs}, as well as of the load voltage U_{Cind}, depend on the inductance value L_{dc} and on the equivalent resistance of the resonant circuit in the inverter diagonal. The transients are simulated for the mode of inductance detuning.

IV. CONCLUSION

The work of a stand alone current fed inverter, as well as of a current fed inverter together with a DC-DC BUCK regulator, has been investigated. A parametric analysis of hysteresis current controlled DC-DC BUCK regulator is performed. It is shown that the regulator represents a current source for a wide enough range of the load variation.
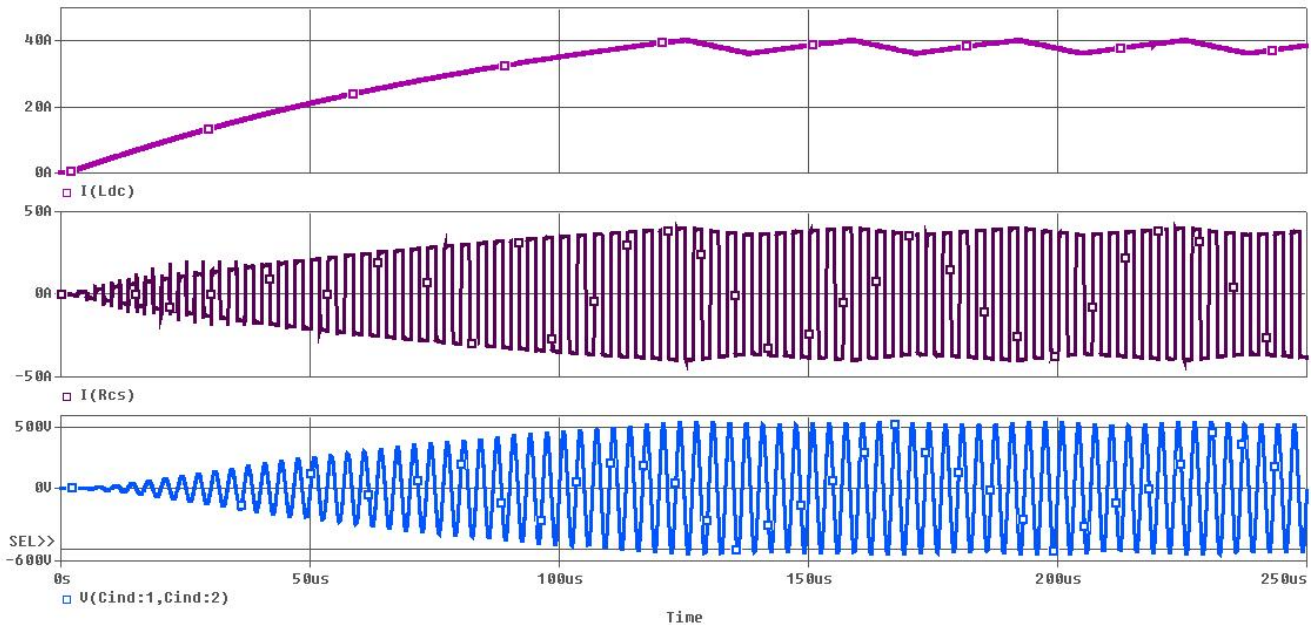
Fig.8. The results from the investigation of the transients in the working together hysteresis current controlled DC-DC BUCK regulator and CFI

The frequency characteristic is investigated of the CFI, supplied by a current source. It is proved, that the voltage on the resonant circuit of the inverter has the same shape as the module of its impedance. The work of CFI is simulated for the modes of capacitance and inductance detuning, from the viewpoint of the commutation processes in the inverter. As a result of simulation, a work in the mode of inductance detuning is recommended, when the commutation losses in semiconductor devices are smaller. The transients of the basic currents and voltages are simulated for the DC-DC BUCK regulator together with the CFI.

V. ACKNOWLEDGEMENT

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